An InGaSb p-channel FinFET

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Abstract

We demonstrate the first InGaSb p-channel FinFET. Towards this goal, we have developed a fin dry-etch technology which yields fins as narrow as 15 nm with vertical sidewalls, an aspect ratio greater than 10 and low sidewall interface state density. We have also realized Si-compatible ohmic contacts with ultra-low contact resistivity of $3.5\cdot10^{-8}$ Ω·cm^2. InGaSb FinFETs with fin widths down to 30 nm and gate lengths down to 100 nm have been fabricated. The Al_2O_3 gate oxide has an EOT of 1.8 nm. A high g_m of 122 μS/μm is obtained in devices of W_f = 100 nm and L_g = 100 nm. In the smallest devices with W_f = 30 nm and L_g = 100 nm, a g_m of 78 μS/μm is achieved.

Introduction

Recently, III-V multigate MOSFETs have attracted much interest for integration into future CMOS technology because of their extraordinary transport and scaling properties [1]. In particular, InGaAs n-type FinFETs and nanowire MOSFETs with promising performance have been reported [2-5]. On the other hand, progress in III-V p-channel transistors is lagging. Among all III-V semiconductors, the antimonide system, $In_xGa_{1-x}Sb$ with $0<x<1$, is most promising due to its high hole mobility and its strong response to compressive stress [1,6]. Planar InGaSb HEMT [7] and MOSFET [8,9] prototypes have been demonstrated with outstanding characteristics. Remarkable improvements have been reported when uniaxial compressive strain is applied [7]. In order to deploy InGaSb in a future generation of CMOS technology, a 3D structure is necessary. In this work, we demonstrate the first InGaSb p-channel FinFET. To achieve this goal, we have developed two critical technologies: a high-aspect ratio dry-etch technology that yields fins as narrow as 15 nm with vertical sidewalls and low sidewall interface state density. We have also realized Si-compatible ohmic contacts with ultra-low contact resistivity of $3.5\cdot10^{-8}$ Ω·cm^2.

Process Development

Antimonide fin etch with nanometer-scale precision and high aspect ratio has never been demonstrated before. The recent achievement of high aspect ratio vertical nanowires and fins in the InGaAs system [10] suggests this technology to be viable. For the InGaSb system, we have developed an RIE process using ICP plasma, a BCl_3/N_2 chemistry and HSQ as the etch mask. **Fig. 1** shows that the etching profile is strongly impacted by the substrate temperature during etch, with a higher etch rate, a more vertical profile and a smoother field being obtained at 250°C. The optimized RIE process yields vertical (>88°) InGaSb nanowires and fins with smallest diameter/width of 15 nm and dense fin arrays with a spacing of 20 nm (**Fig. 2**). The fins have aspect ratio ≥ 10, smooth sidewalls, and no undercutting or trenching.

In order to characterize the electrical quality of the RIE fin sidewalls, a core element of a FinFET, we have fabricated double-gate fin-sidewall capacitors on a p-type GaSb substrate (N_a = $1.5\cdot10^{17}$ cm^{-3}), as shown in **Fig. 3**. Immediately after fin RIE, the sidewalls are cleaned by 1:10 HCl:H_2O solution for 30 s, followed by deposition of 4 nm of ALD Al_2O_3. A planarization step using spin-on-glass and etch-back is performed in order to float the gate on the substrate. Fig. 3 shows C-V measurements at different frequencies on a device with W_f = 60 nm. We estimate a minimum D_{it} = $4.2\cdot10^{11}$ eV^{-1}·cm^{-2} by the conductance method. This promising result is consistent for devices of various W_f, and with earlier reports on planar structures [9]. **Fig. 4** shows sharper C-V characteristics as W_f decreases, as expected.

The second critical element for high-performance InGaSb MOSFETs is a Si-compatible low-resistance ohmic contact scheme. In earlier work we found Ni/Pt/Au as a promising contact scheme to p^+-InAs [11]. Here we have investigated ohmic contacts using either Ni alone or a Ni/Ti/Pt/Al stack. **Fig. 5** shows contact resistance measurements using a circular TLM test structure with a Ni/Ti/Pt/Al (15/10/15/100 nm) contacts on p^+-InAs/$InAs_{0.85}Sb_{0.15}$ 5/30 nm bilayer cap (N_A = $1\cdot10^{19}$ cm^{-3}). A minimum contact resistivity of $3.5\cdot10^{-8}$ Ω·cm^2 is obtained after 1 min annealing at 400°C. This is the first demonstration of Si-compatible contacts to p^+-InAs with ultra-low contact resistivity.

InGaSb FinFET Fabrication

Fig. 6 shows the starting heterostructure. It consists of a 10 nm $In_{0.27}Ga_{0.73}Sb$ quantum-well channel on an

$AlAs_{0.16}Sb_{0.84}$ buffer grown by MBE on (100) SI-GaAs. There is a Be delta-doped layer (10^{12} cm^{-2}) 5 nm underneath the channel. **Fig. 7** shows the process flow. A 15 nm-thick Ni contact layer is first patterned by e-beam lithography and lift-off and then covered by 30 nm of PECVD TEOS. After mesa etch, gate e-beam lithography and TEOS etch, the p^+-InAs cap is selectively recessed in a citric acid/H_2O_2 solution. Fins are then patterned by e-beam lithography and etched using HSQ as the mask. This is immediately followed by deposition of 4 nm of Al_2O_3 by ALD at 250°C and sputtering of 45 nm of Mo which serves as gate metal. The Ti/Au gate head is then defined by e-beam lithography, followed by Mo dry etch. This result in a gate that is self-aligned to the p^+ cap. Finally, 40 nm of TEOS is deposited and large contact pads are formed through contact vias, to reduce leakage. The HSQ fin mask remains till the end of the process, resulting in a double-gate geometry.

A typical FinFET consists of 60-70 fins with W_f between 30 and 100 nm. The gate length (L_g) ranges between 100 nm and 1 μm. The total fin height is 150 nm. **Fig. 8** illustrates the device geometry. **Fig. 9** shows a FIB cross-sectional image of the intrinsic portion of a device with W_f=30 nm.

FinFET Results

Fig. 10 shows output and transfer characteristics of a typical InGaSb FinFET with W_f=30 nm and L_g=100 nm. **Fig. 11** shows typical output characteristics of a wider fin device. The narrow fin devices exhibit better saturation behavior for all channel lengths. All devices suffer from poor turn off. Scaling and orientation dependence studies suggest that much of the leakage current flows through the fin. Furthermore, high δ-doping combined with sidewall interface states also prevent effective turn-off, which is mitigated at low temperature (**Fig. 12-13**). Therefore, further optimization of the heterostructure design and growth conditions is needed. It is also critical to study techniques to reduce sidewall roughness in antimonide heterostructure fins.

The scaling behavior of our devices is shown in **Figs. 14-17**. Linear V_T, extracted using the extrapolation method, shows the beneficial effect of W_f scaling on short-channel effects (**Fig. 14**). The devices also show a well-behaved dependence of g_m on L_g and W_f. (**Fig. 15**). The highest g_m of 122 μS/μm is obtained in devices with W_f=100 nm and L_g=100 nm (normalized by twice the channel thickness). g_m degrades as W_f decreases. The measurement of R_{on} (at V_{GS}=-2.5 V) and extraction of R_{SD} (both normalized as in g_m) suggest that g_m degradation with W_f is due to an increase in R_{sd} as W_f is reduced (**Figs. 16, 17**).

Fig. 18 shows the impact of fin orientation on g_m. A strong orientation dependence is observed with devices with fins oriented along the $[01\bar{1}]$ direction being the best, those along [001] and [010] being the worst, and [011] being somewhere in between. A similar dependence is obtained for all L_g and W_f. This parallels p-InGaAs QWFETs under uniaxial compressive stress [12]. This suggests that the as-grown biaxial compressive stress in the pseudomorphic InGaSb channel has relaxed along the direction transversal to the fin leaving being a strong anisotropic strain distribution.

Fig. 19 benchmarks g_m vs. L_g among published InGaSb p-MOSFETs. As the first FinFETs in this material system, the results that have been obtained are very encouraging.

Conclusions

InGaSb FinFETs are demonstrated for the first time. Devices with fin widths down to 30 nm and gate lengths down to 100 nm have been fabricated with promising electrical characteristics. This important result arises from new process development of high-aspect ratio fin etching technology with low interface-state density sidewalls and Si-compatible ohmic contacts with ultra-low contact resistivity. This work highlights the potential of InGaSb p-channel multigate MOSFETs for future logic applications.

Acknowledgements

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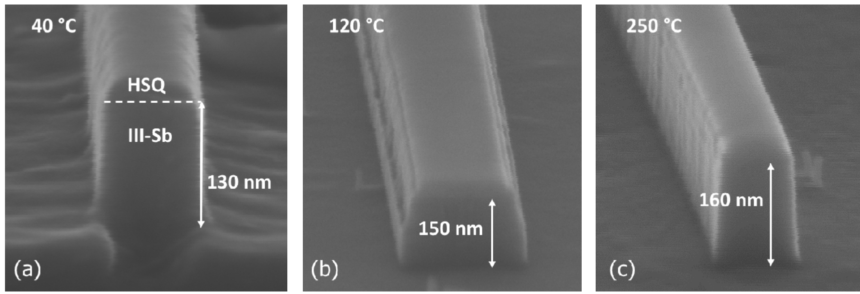


Fig.1: Reactive ion etching of antimonide-based heterostructures using HSQ hard mask at: (a) 40°C, (b) 120°C, and (c) 250°C substrate temperature during etching.

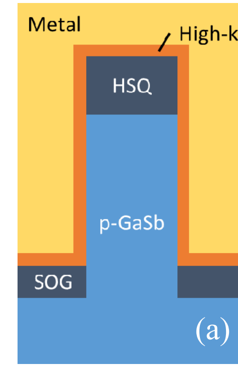


Fig. 3: (a) p-GaSb fin sidewall capacitor; (b) C-V characteristics of 4 nm Al_2O_3/p-GaSb sidewall capacitor with 60 nm fins. Inset: D_{it} extraction by the conductance method.

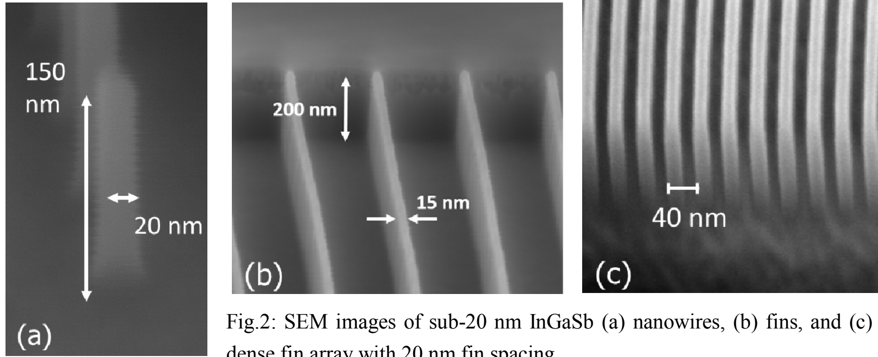
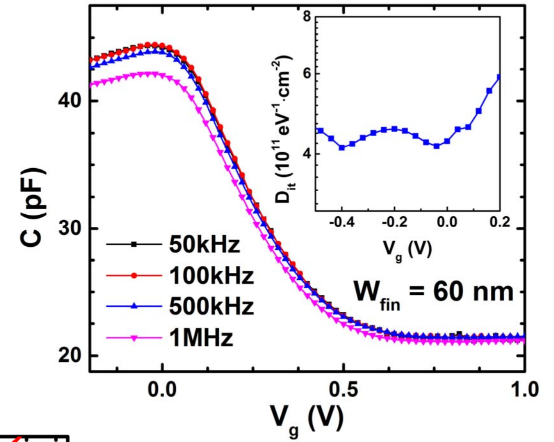


Fig.2: SEM images of sub-20 nm InGaSb (a) nanowires, (b) fins, and (c) dense fin array with 20 nm fin spacing.



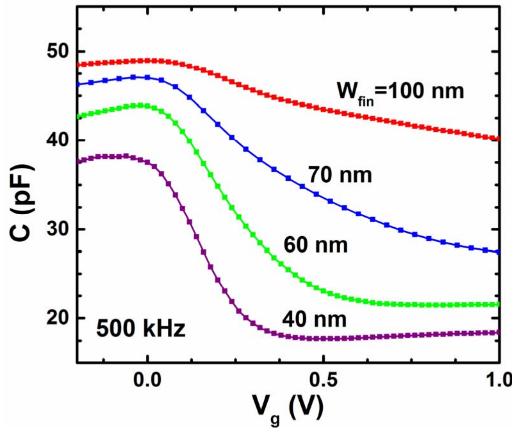


Fig. 4: C-V characteristics of 4 nm Al_2O_3/p-GaSb sidewall capacitors of various fin widths.

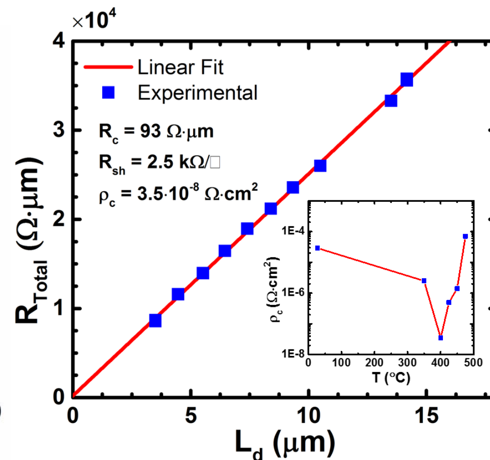


Fig. 5: Si-compatible Ni/Ti/Pt/Al ohmic contacts to p^+-InAs measured by circular TLM. Inset: ρ_c evolution vs. annealing temperature in sequential annealing experiments.

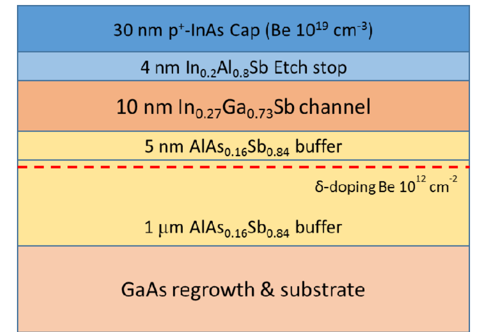


Fig. 6: Starting heterostructure, grown by MBE, for InGaSb FinFET fabrication.

- 15 nm Ni ohmic contact patterned by EBL
- PECVD 30 nm TEOS
- Gate EBL, TEOS dry etch
- Mesa photolithography, TEOS dry etch
- Cap layer wet etch by 10:1 citric acid/H_2O_2
- Fin EBL and 150 nm dry etch
- ALD 4 nm Al_2O_3 gate dielectric
- Sputter 45 nm Mo gate metal
- Gate head (Ti/Au) EBL, Mo dry etch
- PECVD 40 nm TEOS
- Contact via opening by EBL and dry etch
- Pt/Au deposition and S/D pad formation

Fig. 7: Process flow for InGaSb FinFETs.

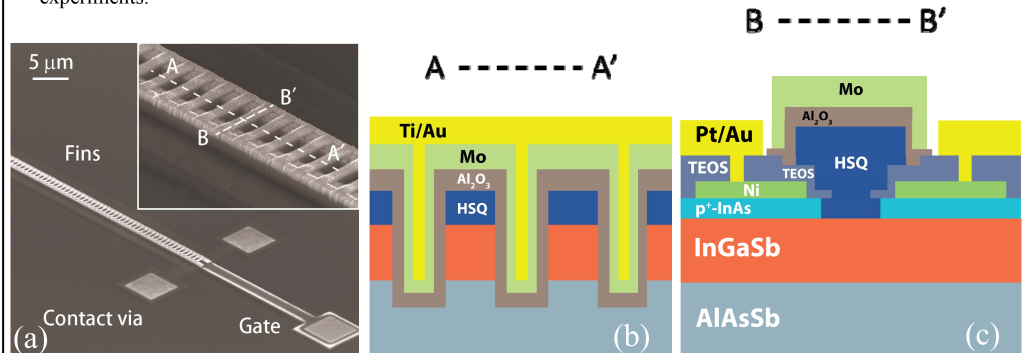


Fig. 8: (a) SEM image of an InGaSb FinFET before final pad deposition. Inset: zoom-in of the gate region. Device cross-sectional structure along (b) A-A' and (c) B-B' directions.

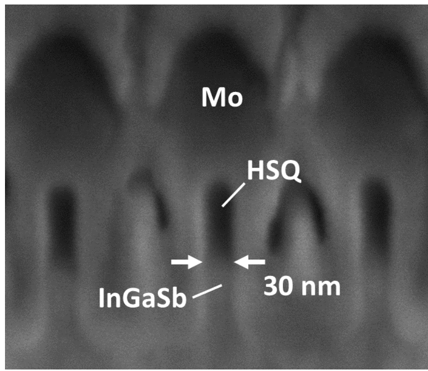
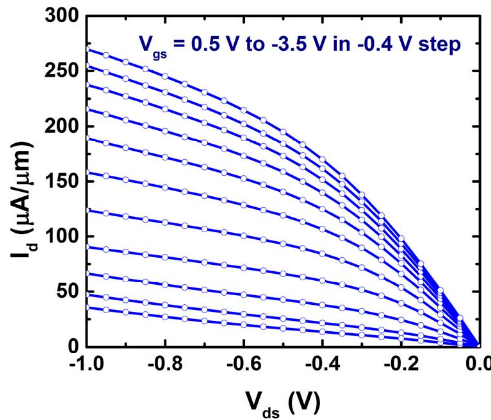


Fig. 9: FIB cross-section of finished InGaSb FinFET with W_f=30 nm.



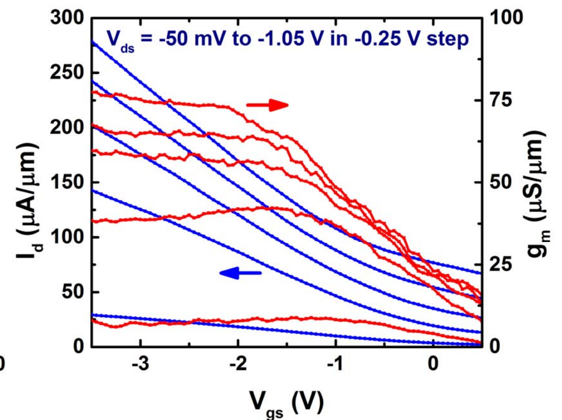


Fig. 10: Output and transfer characteristics of InGaSb FinFET with W_f=30 nm and L_g=100 nm.

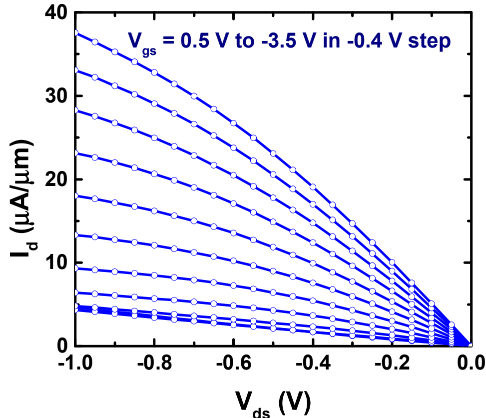


Fig. 11: Output characteristics of InGaSb FinFET with W_f=100 nm and L_g=1 μm.

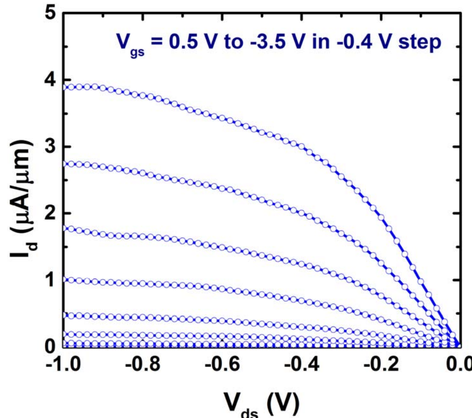


Fig. 12: Low temperature (77K) output characteristics of FinFET with W_f=30 nm and L^g=300 nm.

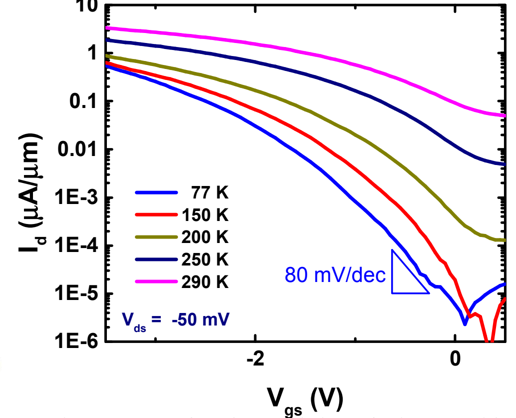


Fig. 13: Transfer characteristics of FinFET with W_f=30 nm and L_g=300 nm at different temperatures (V_{DS}=-50 mV).

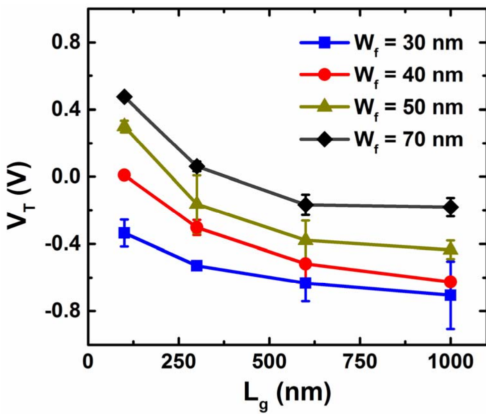


Fig. 14: Linear V_T roll off with gate length of InGaSb FinFETs with various fin widths.

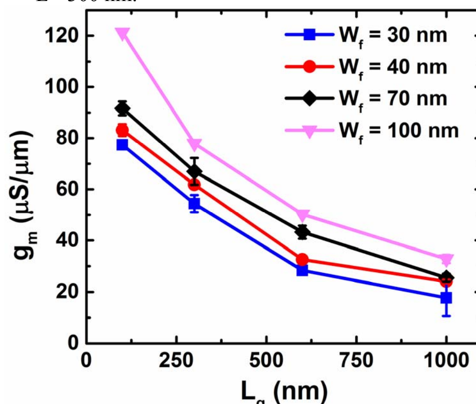


Fig. 15: Maximum g_m as a function of L_g for devices with different fin widths (along $[01\bar{1}]$).

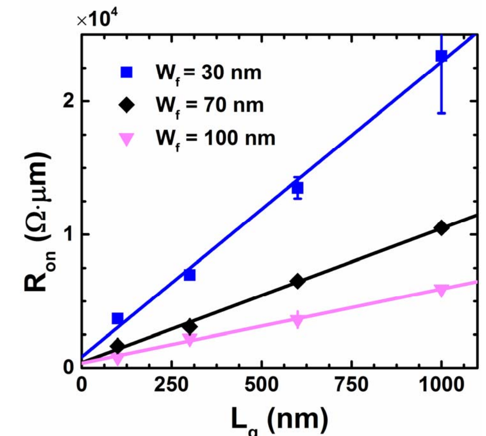


Fig. 16: Access resistance extraction of devices with various W_f at V_{GS}=-2.5V.

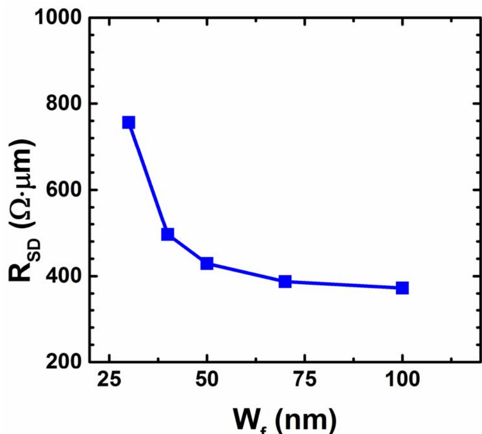


Fig. 17: Access resistance as a function of InGaSb fin width.

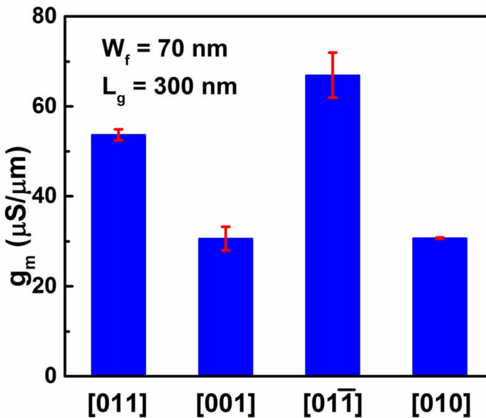


Fig. 18: Dependence of maximum g_m on fin orientation for devices with W_f=70 nm, L_g=100 nm.

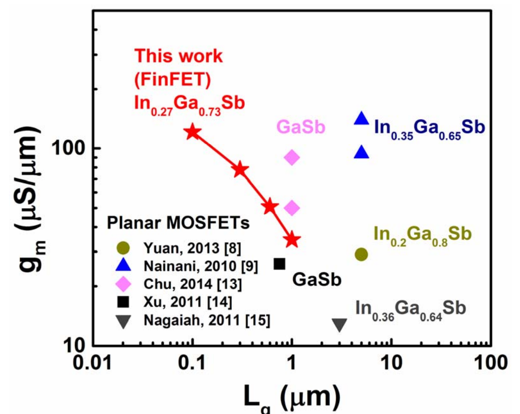


Fig. 19: Maximum g_m vs. L_g of recently published InGaSb MOSFETs.